

## INFORMATION DISCLOSURE CITATION

ATTY. DOCKET NO.

**SERIAL NO.**

540-127

09/152,266

APPLICANT

CAMPBELL

(Use several sheets if necessary)

FILING DATE

GROUP

September 14, 1998

2773

## U.S. PATENT DOCUMENTS

[illegible]

## FOREIGN PATENT DOCUMENTS

[illegible]

**OTHER DOCUMENTS** (including Author, Title, Date, Pertinent pages, etc.)

*Examiner	Thomas Hamer	Date Considered	5/2/03	

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to application.

Form PTO-FB-A820 (Also PTO-1449)

# INFORMATION DISCLOSURE CITATION

ATTY. DOCKET NO.

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(To Be Assigned)

APPLICANT

CAMPBELL et al

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(Use several sheets if necessary)

14 September 1998

## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
TP	5,265,203	11/23/1993	PEASLEE et al			
TP	4,964,040	10/16/1990	WILCOX			
TP	4,905,175	2/27/1990	CORBETT et al			
TP	4,468,727	8/28/1984	CARRISON et al			

## FOREIGN PATENT DOCUMENTS

DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO
TP	0 362 903 A	4/11/1990			X
TP	WO 91 16681 A	10/31/1991			X
TP	0 364 000 A	4/18/1990			X

## OTHER DOCUMENTS (including Author, Title, Date, Pertinent pages, etc.)

	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 28, no. 5, October 1985, NEW YORK US, pages 1981-1985, XP002034326 "Procedure for Hierarchical Chip Physical Design" see the whole document.
	IEICE TRANSACTIONS ON ELECTRONICS, vol. E76-C, no. 11, November 1993, pages 1641-1648, XP000424603 NOBUTAR SHIBATA ET AL.: "HIGH-PERFORMANCE MEMORY MACROCELLS WITH ROW AND COLUMN SLICEABLE ARCHITECTURE" see abstract see page 1652, left-hand column, line 23; figures 1,2

*Examiner	Thomas pham	Date Considered	5/2/03
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